REMARKS

Claims 1-12 were examined and reported in the Office Action. Claims 1-5 are rejected. Claims 1-4 are amended. Claims 1-12 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103

A. It is asserted in the Office Action that claims 1-5 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Fanning et al. ("Fanning") in GaAs Mantech Conference Article, in view of U. S. Patent No. 5,034,608 issued to Tavrow et al. ("Tavrow").

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "[a] semiconductor device comprising: a semiconductor substrate; source and drain electrodes, which are formed on the semiconductor substrate to make ohmic contact with the semiconductor

substrate; a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Fanning discloses a dielectrically defined gate process using optical lithography to pattern T-gates. Fanning discloses a silicon nitride layer formed on a substrate, drains and source electrodes formed on the silicon nitride layer, and a T-gate formed between the source and drain electrodes. Fanning, however, does not teach, disclose or suggest "a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Tavrow discloses an infrared sensor operable without cooling. Tavrow discloses that a MOS transistor is insulated with an insulator, such as aerogel. Tavrow, however, does not teach, disclose or suggest "a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Even if Fanning is combined with Tavrow, the resulting invention would still not teach, disclose or suggest "a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Further, Applicant submits that by viewing the disclosure of Fanning combined with Tavrow, one can not jump to the conclusion of obviousness without impermissible hindsight. According to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to have "a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Neither Fanning, Tavrow, nor the combination of the two teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above. Since neither Fanning, Tavrow, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's claim 1, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 1 is not obvious over Fanning in view of Tavrow since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from claim 1, namely claims 2-5, would also not be obvious over Fanning in view of Tavrow for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-5 are respectfully requested.

B. It is asserted in the Office Action that claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over P1997-0018657 issued to Moon et al ("Moon"), in view of Tavrow et al.

Tavrow is discussed above in section I(A) regarding claim 1.

Moon discloses a method for forming a T-gate electrode by forming an insulating layer on a substrate, forming source and drain electrodes by removing the insulation layer. Moon, however, does not teach, disclose or suggest "a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Therefore, even if Moon is combined with Tavrow, the resulting invention would still not teach, disclose or suggest "a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Further, Applicant submits that by viewing the disclosure of Moon combined with Tavrow, one can not jump to the conclusion of obviousness without impermissible hindsight. Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to have "a T-shaped gate electrode, which is formed between the source and drain electrodes on the semiconductor

substrate; a first insulating layer formed on the semiconductor substrate; a silica aerogel layer formed on the first insulating layer; and a second insulating layer formed on the silica aerogel layer, the source electrode and the drain electrode, the second insulating layer including silica aerogel, the second insulating layer is coupled to the T-shaped gate electrode."

Neither Moon, Tavrow, nor the combination of the two teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above. Since neither Moon, Tavrow, nor the combination of the two teach, disclose or suggest all the limitations of Applicant's claim 1, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's claim 1 is not obvious over Moon in view of Tavrow since a *prima facie* case of obviousness has not been met under MPEP §2142.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claim 1 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-12 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: January 5, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on January 5, 2005.

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Jean Svoboda